REMARKS

The Office Action mailed November 30, 2001, has been received and its contents carefully noted.

In order to advance the prosecution, claims 1 and 7 have been amended to more particularly point out the invention. Claims 1-4 and 7-10 are pending in the application.

Drawings

Also, as part of Applicant's response, attached hereto are copies of Figures 3 and 5A with proposed drawing changes shown in red. The Examiner is requested to review and approve these changes which were made at his suggestion.

Claim Rejections - 35 USC § 102

The Examiner rejected claims 1-4 and 7-10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No.5,534,927 to Shishikui et al. It is respectfully submitted that the present claimed invention is patentable over the art of record for the following reasons. Accordingly, reconsideration of the Examiner's rejection is requested.

Claim 1 and 7 are further amended such that moving-picture signal portions in specific frames or fields carried by the input moving picture signal are encoded by intra- or inter-picture coding in main coding, and the same moving-picture signal

portions are encoded by only intra-picture coding in subsidiary coding.

The newly added term "moving-picture signal portions" is based on an input moving picture signal which is subjected to main and subsidiary coding (page 7, lines 11 to 13) for each moving-picture signal portion.

The Examiner alleged that Shishikui et al, in FIGS. 2 and 9, disclose the claimed apparatus and method, under 35 U.S.C. 102(b).

In FIG. 2, the controller 52 compares a block of the current image signal with a prediction error signal to generate either an intra mode or an intermode (column 6, lines 1 to 7). SD-DCT processing is performed in the intra mode while 1D-DCT processing is performed in the inter mode (column 6, lines 33 to 38).

In Shishikui et al, whether the image signal is subjected to the 2D- or 1D-DCT processing is decided by the controller 52 in accordance with the results of comparison.

On the contrary, in the present claimed invention, the input signal is always subjected to both main and subsidiary coding.

In Shishikui et al, the image signal goes though the 2D-DCT processing in block or 8 x 8 pixel units (column 6, lines 39 to 41). Additionally, the image signal goes though the 1D-DCT processing in each of eight 8 x 1 pixels sub-blocks (column 6, lines 52-55).

On the contrary, in the present claimed invention, the same moving-picture signal portions of the input moving picture signal are subjected to the main and subsidiary coding.

In FIG. 9 of Shishikui et al, the input signal is separated into horizontal high and low frequency components. Each frequency component is further separated into vertical high and low frequency components. The vertical high frequency component goes though the 1D-DCT processing while the vertical low frequency component goes though the 2D-DCT processing (column 9, lines 36 to column 10, line 22).

The same coding technique is discussed in BACKGROUND ART OF THE INVENTION in the present invention.

Moreover, in the present claimed invention, the same moving-picture signal portions of the input moving picture signal are subjected to the main and subsidiary coding. The same moving-picture signal portions are the signal portions at the same frequency.

As discussed, Shishikui et al., discloses coding processing for each spatial frequency component for high coding efficiency.

In contrast, the present claimed invention allows decoding of subsidiary bitstreams in frames or fields because the subsidiary coding is only intra-picture coding, thus achieving quick video reproduction in random access or channel switching. Moreover, the present invention achieves decrease in total code

amount in both main and subsidiary coding because only specific frames or fields of the picture signal are subjected to the intra-picture coding in the subsidiary coding.

More specifically, amended claim 1 recites an apparatus for efficiently coding a moving picture signal. The apparatus has a main coding processor to selectively encode an input moving picture signal by intra-picture coding or inter-picture coding in unit of frame or field output a main bit stream. A subsidiary coding processor is recited to encode motion-picture signal portions in specific frames or fields carried by the input moving picture signal by only intra-picture coding to output a subsidiary bit stream. The same motion-picture signal portions being also coded by the inter-picture coding by the main coding processor. Additionally, there is recited a multiplexer to multiplex the main and subsidiary bit streams so that the subsidiary bit streams for which the motion-picture signal portions have been encoded only by the intra-picture coding by the subsidiary coding processor are periodically inserted in the main bit stream for which same motion-picture signal portions have also been encoded by the inter-picture coding by the main coding processor in the vicinity of a predetermined number of the frames or fields coded by the inter-picture coding, thus generating an output bit stream. It is respectfully submitted that the art of record does not teach or suggest these features

and claim 1, as now amended, is patentable.

Amended claim 7 recites a method of efficiently coding a moving picture signal and comprises the step of selectively encoding an input moving picture signal by intra-picture coding or inter-picture coding in unit of frame or field to output a main bit stream. Another step of the method is encoding motion-picture signal portions in specific frames or fields carried by the input moving picture signal by only intra-picture coding to output a subsidiary bit stream. The same motion-picture signal portions are also coded by the inter-picture coding by the selective encoding. Additionally, there is a step of multiplexing the main and subsidiary bit streams so that the subsidiary bit streams for which the motion-picture signal portions have been encoded only by the intra-picture coding are periodically inserted in the main bit stream for which the same motion-picture signal portions have also been encoded by the inter-picture coding in the vicinity of a predetermined number of the frames or fields coded by the inter-picture coding, thus generating an output bit stream. It is respectfully submitted that the art of record does not teach or suggest these steps and claim 7, as now amended, is patentable.

In view of the foregoing amendments and remarks, the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 1-4 and 7-10 to allow these claims and to

find this application to be in allowable condition.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is invited to telephone the undersigned to arrange for such a conference.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

JACOBSON HOLMAN PLLC

By _____
John C. Holman
Reg. No. 22,769

400 Seventh Street, N.W.
Washington, D.C. 20004-2201
(202) 638-6666
Date: February 27, 2002
Atty. Docket: 5970/P63212US0

Version with markings to show changes made.

In the Claims:

Please amend claims 1 and 7 as follows:

1. (Twice Amended) An apparatus for efficiently coding a moving picture signal, comprising:

a main coding processor to selectively encode an input moving picture signal by intra-picture coding or inter-picture coding in unit of frame or field output a main bit stream;

a subsidiary coding processor to encode motion-picture signal portions in specific frames or fields carried by the input moving picture signal by only intra-picture coding to output a subsidiary bit stream, the [specific frames or fields] same motion-picture signal portions being also coded by the inter-picture coding by the main coding processor; and

a multiplexer to multiplex the main and subsidiary bit streams so that the subsidiary bit streams for which the [specific frames or fields] motion-picture signal portions have been encoded only by the intra-picture coding by the subsidiary coding processor are periodically inserted in the main bit stream for which [specific frames or fields] same motion-picture signal portions have also been encoded by the inter-picture coding by

the main coding processor in the vicinity of a predetermined number of the frames or fields coded by the inter-picture coding, thus generating an output bit stream.

7. (Twice Amended) A method of efficiently coding a moving picture signal, comprising the steps of:

selectively encoding an input moving picture signal by intra-picture coding or inter-picture coding in unit of frame or field to output a main bit stream;

encoding motion-picture signal portions in specific frames or fields carried by the input moving picture signal by only intra-picture coding to output a subsidiary bit stream, the [specific frames or fields] same motion-picture signal portions being also coded by the inter-picture coding by the selective encoding; and

multiplexing the main and subsidiary bit streams so that the subsidiary bit streams for which the [specific frames or fields] motion-picture signal portions have been encoded only by the intra-picture coding are periodically inserted in the main bit stream for which the [specific frames or fields] same motion-picture signal portions have also been encoded by the inter-picture coding in the vicinity of a predetermined number of the frames or fields coded by the inter-picture coding, thus generating an output bit stream.